

Layout And Use Of Bond Pads And Probe Pads For Testing Of  
Integrated Circuits Devices  
Atty. Dkt. No. : M-9433 US Inventor: Marian E. Ong  
Sheet 1 of 9

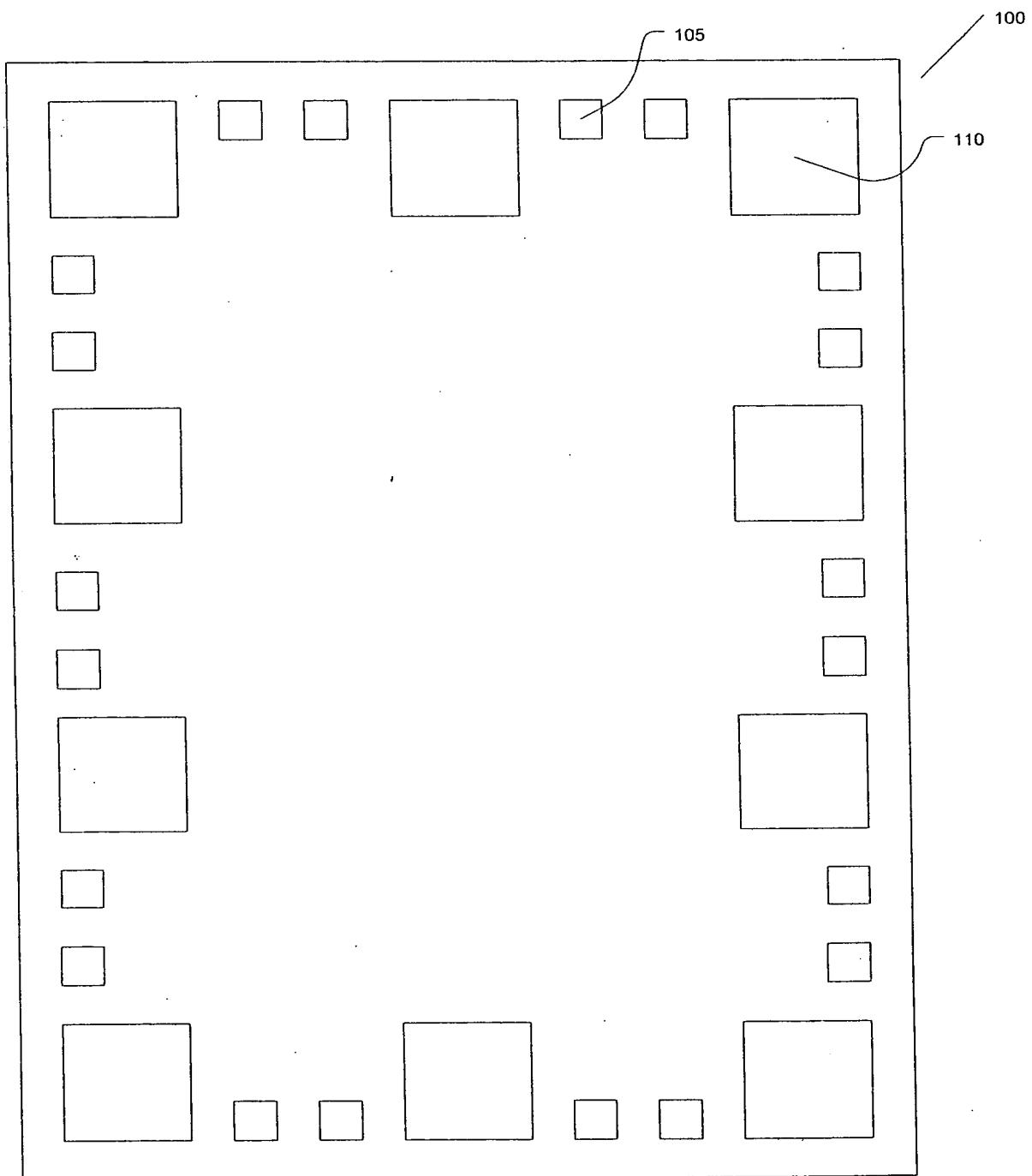


FIG. 1

Layout And Use Of Bond Pads And Probe Pads For Testing Of  
Integrated Circuits Devices  
Atty. Dkt. No. : M-9433 US Inventor: an E. Ong  
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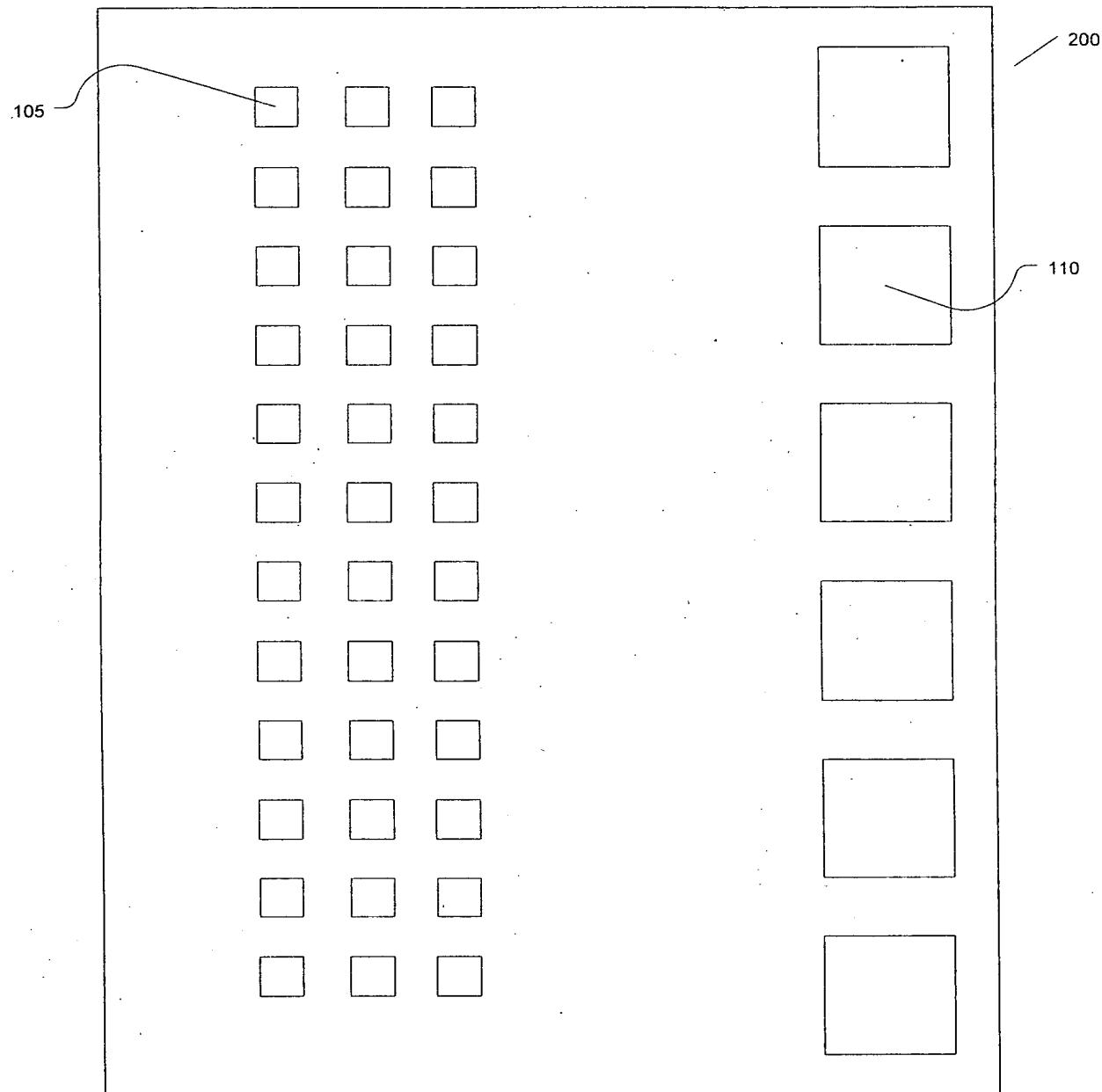


FIG. 2

Layout And Use Of Bond Pads And Probe Pads For Testing Of  
Integrated Circuits Devices  
y. Dkt. No. : M-9433 US Inventor: A. E. Ong  
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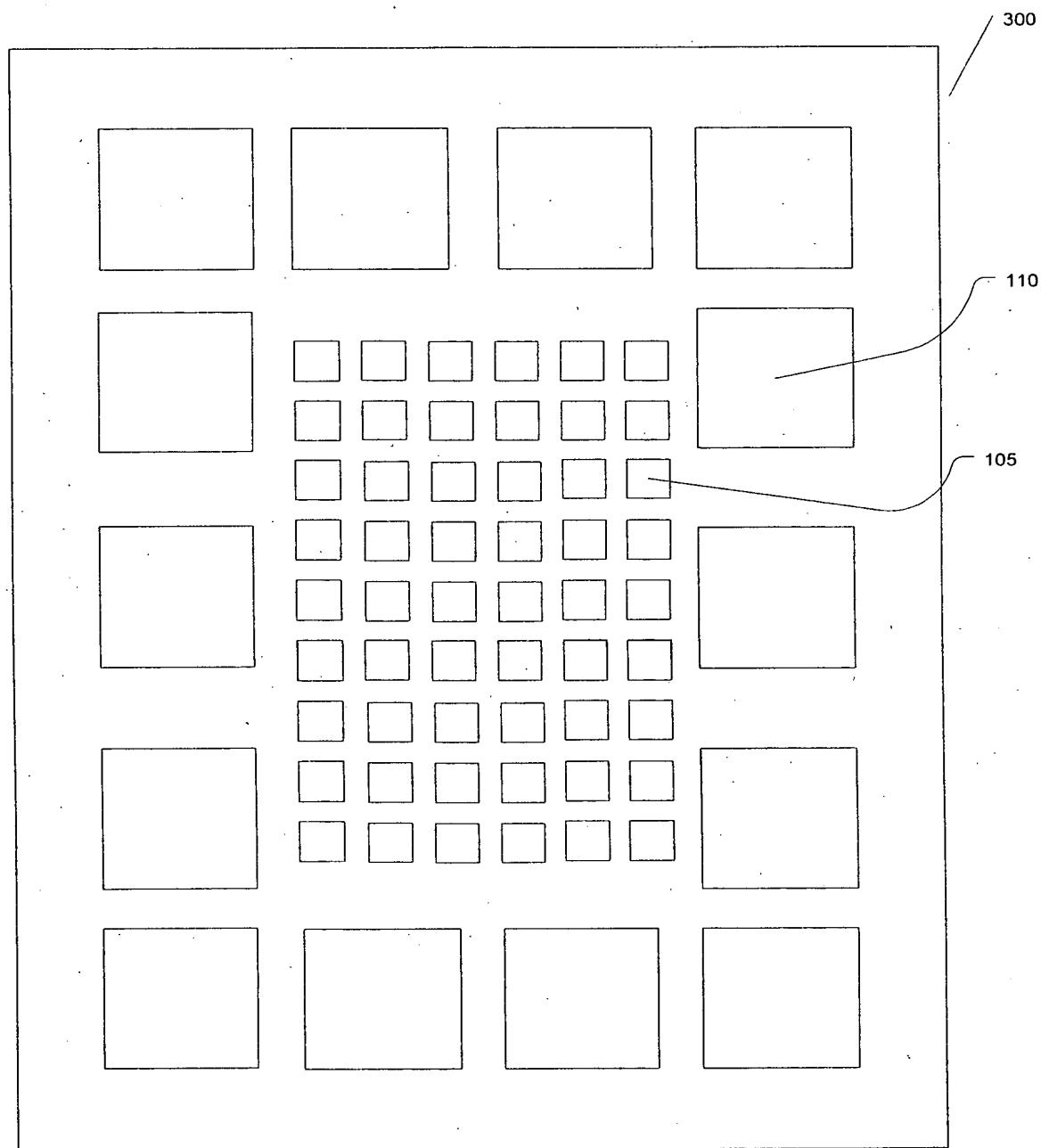


FIG. 3

Layout And Use Of Bond Pads And Probe Pads For Testing Of  
Integrated Circuits Devices  
U.S. Pat. No. : M-9433 US Inventor: Ad... E. Ong  
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140a  
140b  
105a  
105b  
130a  
130b  
110  
120  
400

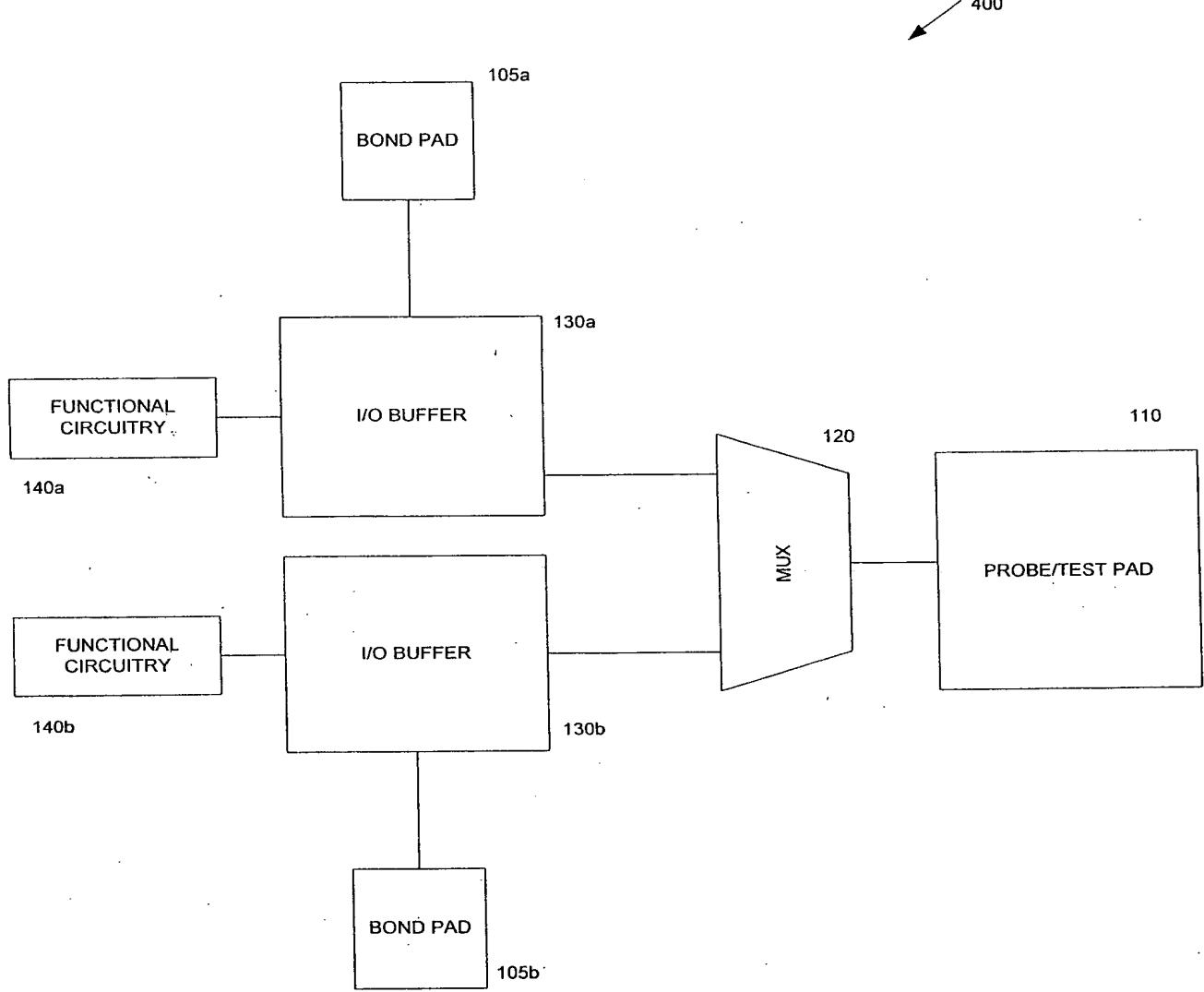


FIG. 4

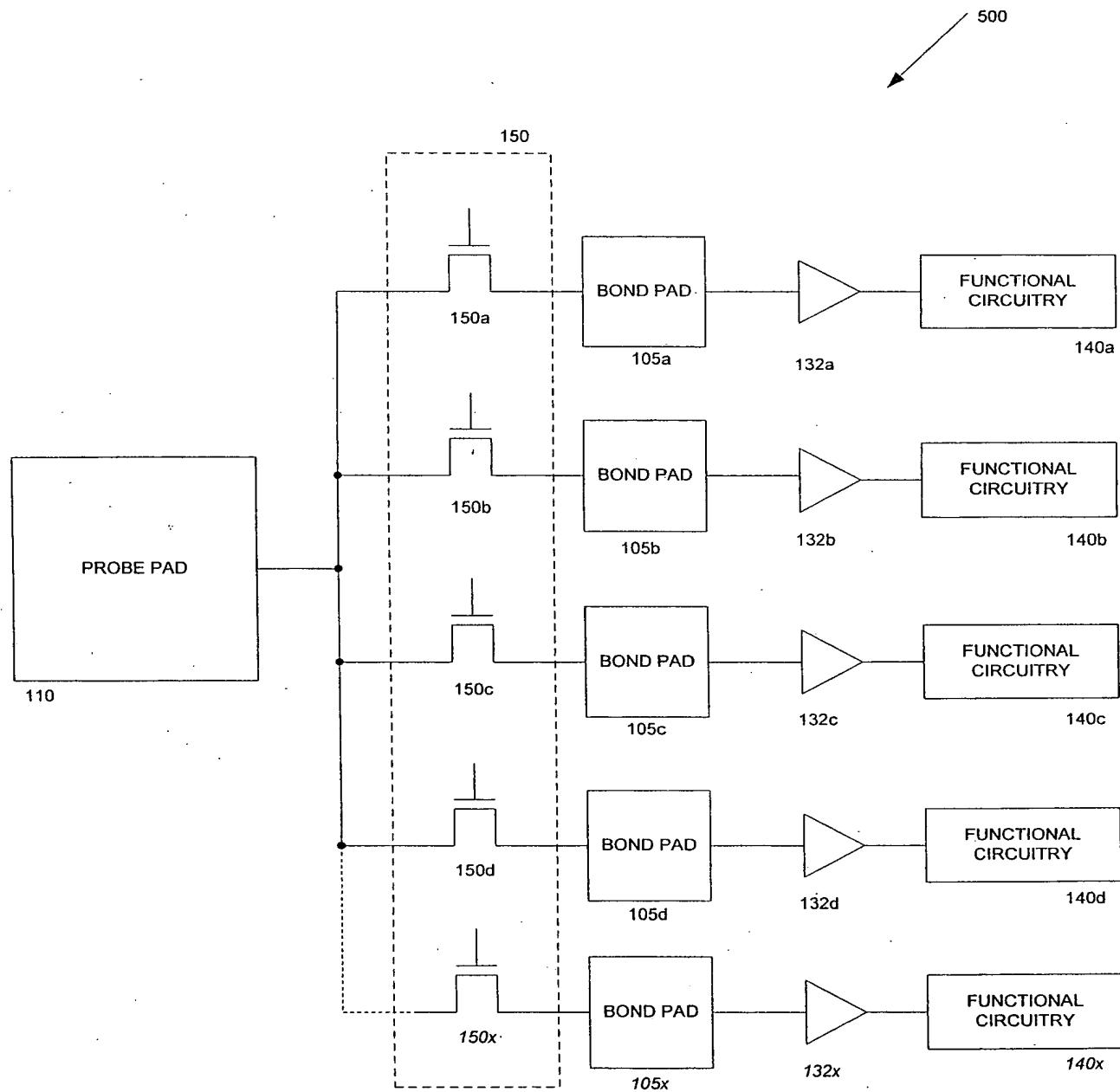


FIG. 5

Layout And Use Of Bond Pads And Probe Pads For Testing Of  
Integrated Circuits Devices  
Atty. Dkt. No. : M-9433 US Inventor: Adrian E. Ong  
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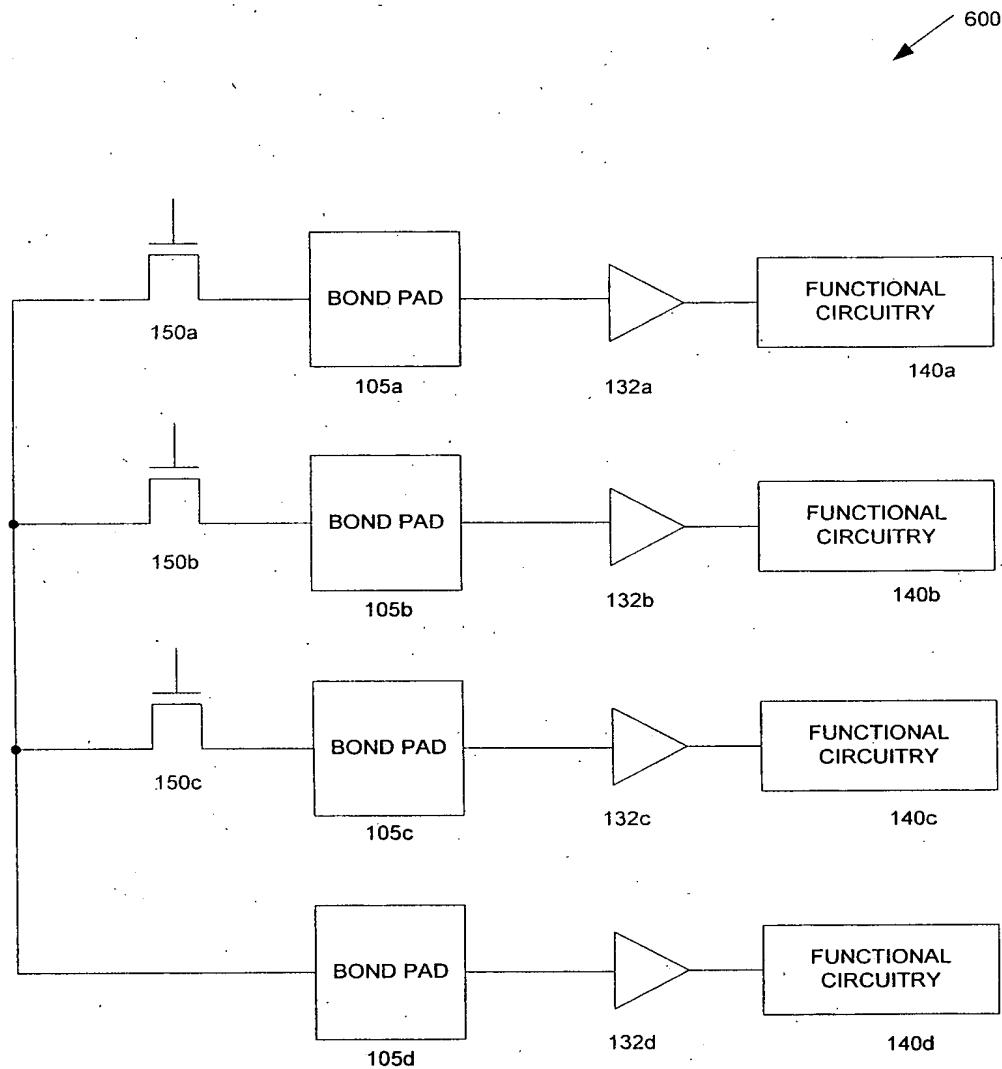


FIG. 6

**Layout And Use Of Bond Pads And Probe Pads For Testing Of  
Integrated Circuits Devices**

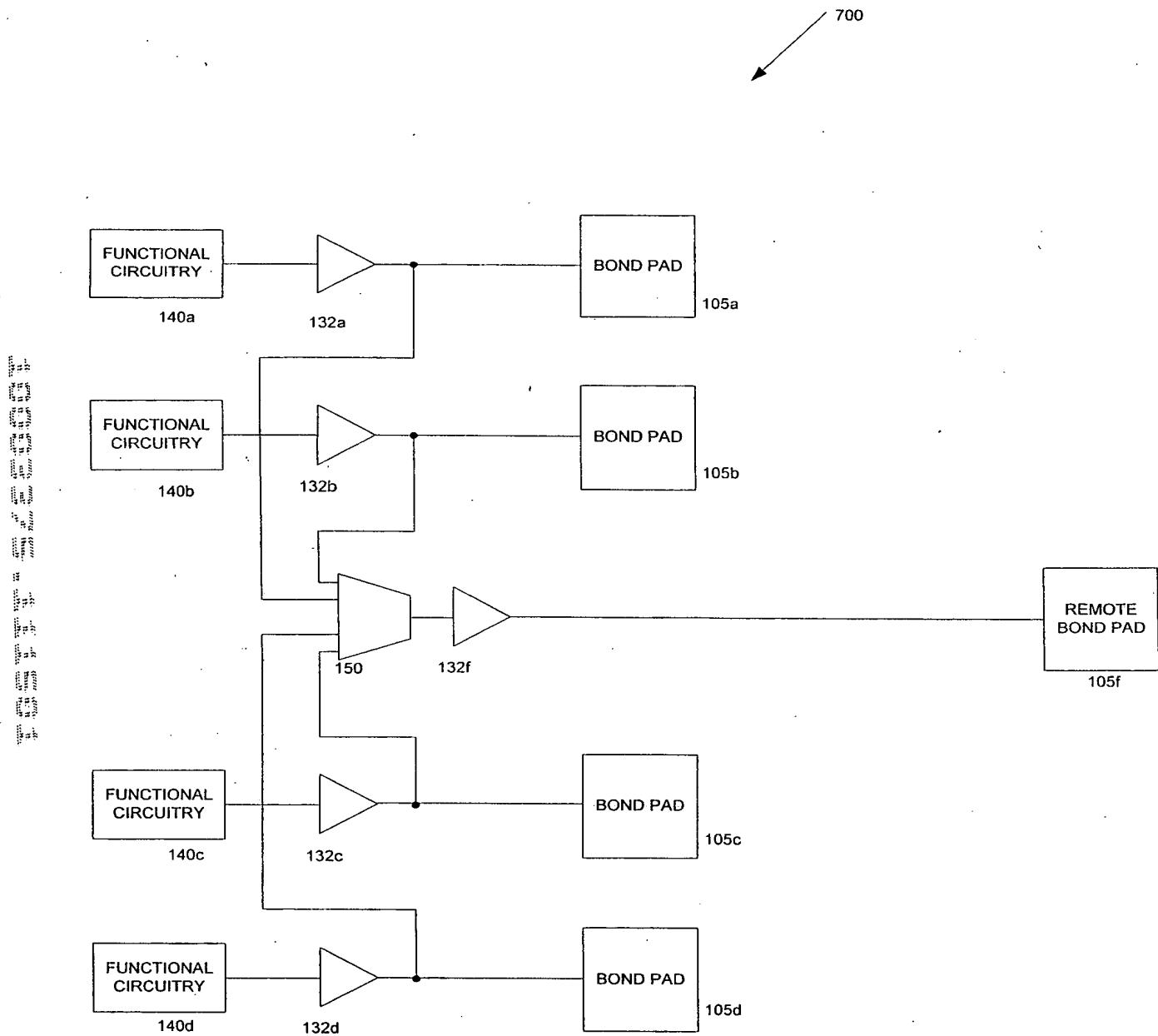


FIG. 7

Layout And Use Of Bond Pads And Probe Pads For Testing Of  
Integrated Circuits Devices  
A. Okt. No. : M-9433 US Inventor: Adriano Ong  
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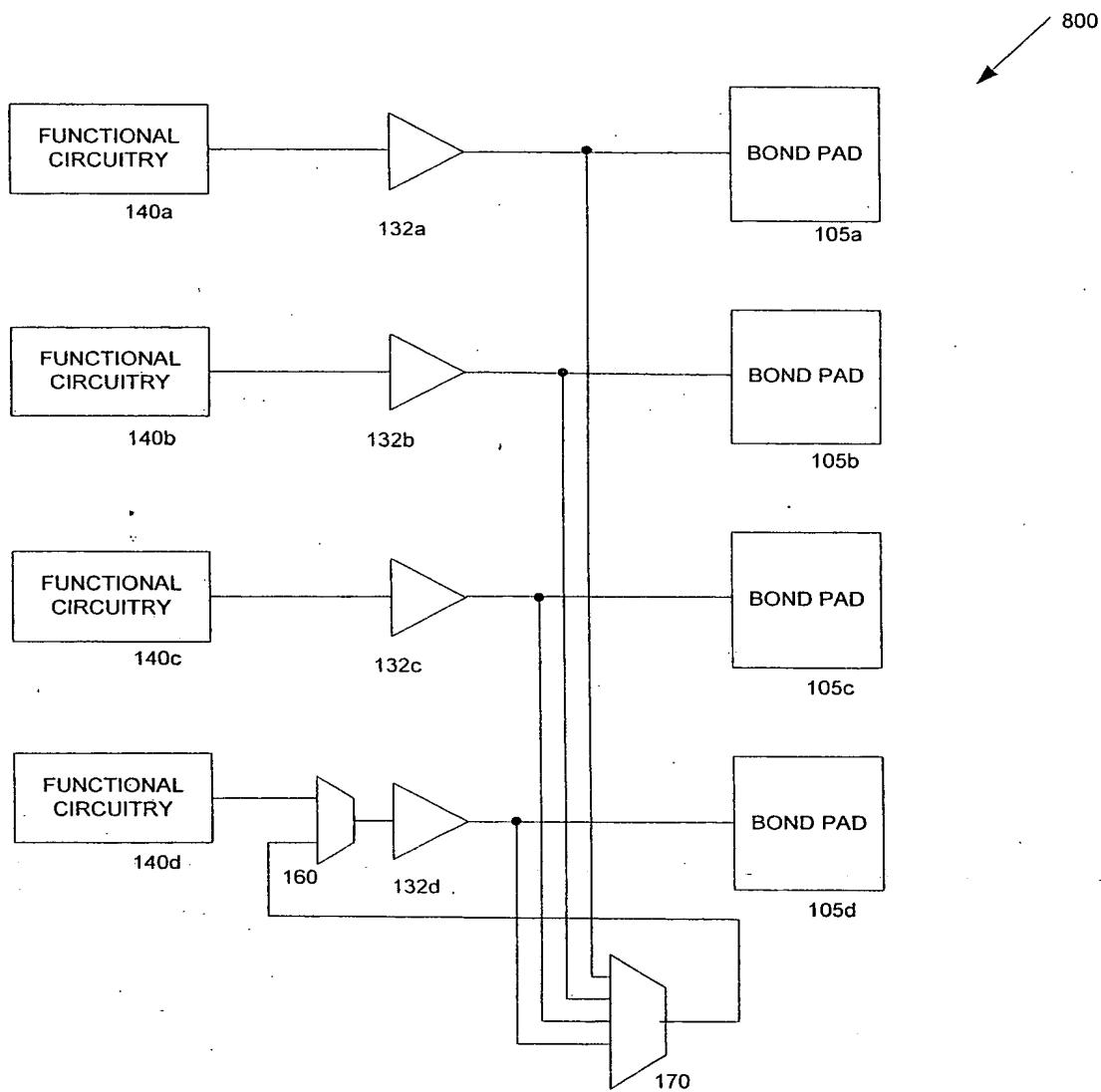


FIG. 8

Layout And Use Of Bond Pads And Probe Pads For Testing Of  
Integrated Circuits Devices  
Dkt. No. : M-9433 US Inventor: Adi [redacted] Ong  
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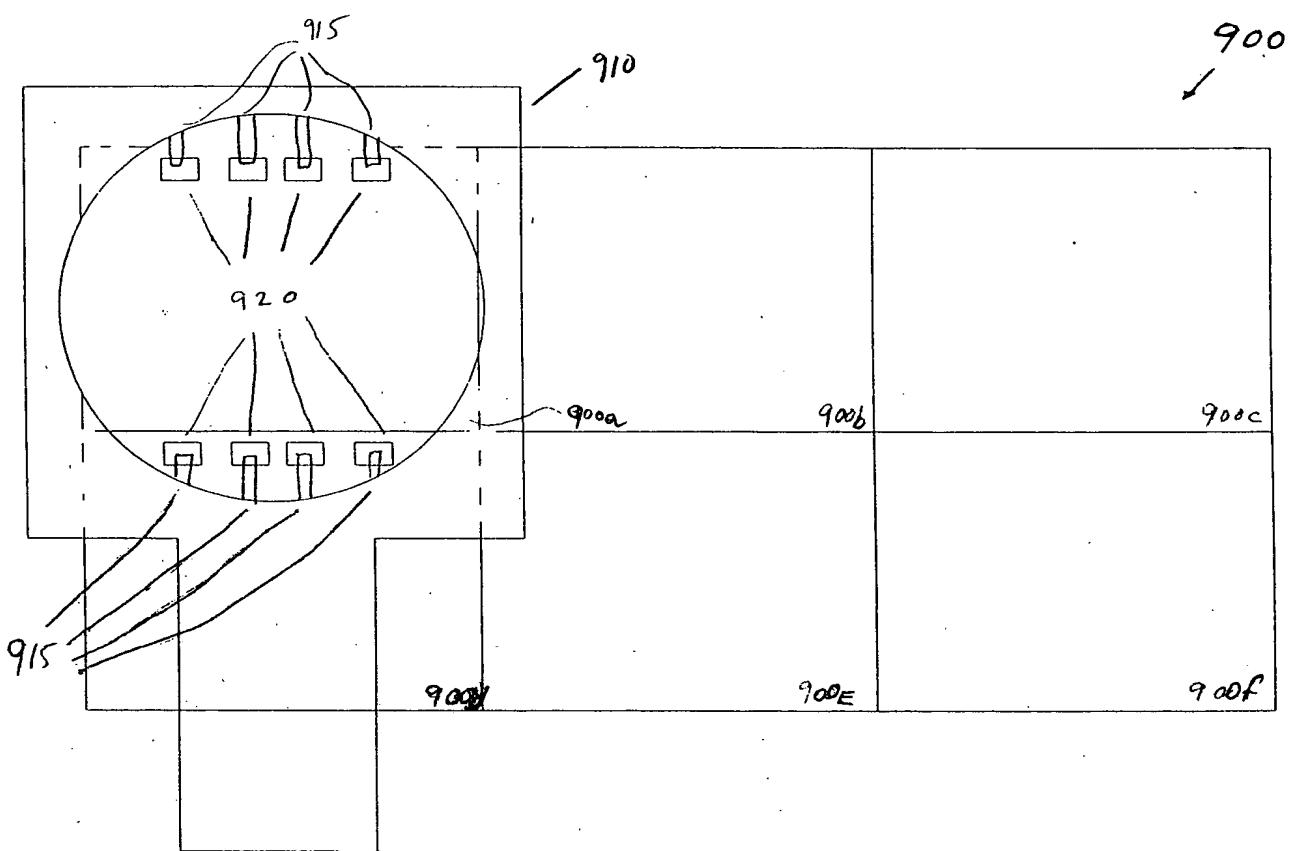


FIG. 9